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Michael Bailey

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EXAMINER

WEST, JEFFREY R

ART UNIT

PAPER NUMBER

2857

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/664,396	Applicant(s) BAILEY ET AL.	
	Examiner Jeffrey R. West	Art Unit 2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 January 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 January 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. Claims 1 and 9 are objected to because of the following informalities:

In claim 1, line 14, to avoid problems of antecedent basis, "said microprocessor" should be ---said at least one microprocessor---.

In claim 9, line 4, to avoid problems of antecedent basis, "said voltage divider" should be ---said voltage divider coupled to said input of said at least one RS232 receiver---.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3, 10, 11 and 16-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 is considered to be vague and indefinite because it attempts to further limit parent claim 1 to include "a voltage divider coupled to said at least one RS232 receiver to reduce a voltage of said constant time reference AC voltage signal to within a detectable range". Parent claim 1, however, specifies "at least one RS232 receiver having an input for receiving an alternating current (AC) voltage input signal" and not a "constant time reference AC voltage signal". Therefore, it is

unclear to one having ordinary skill in the art how a voltage divider coupled to the input of the at least one RS232 receiver can reduce a voltage of a signal not present at the input.

Claims 10 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being vague and indefinite because they make reference to "said voltage divider coupled to said input of said RS232 receiver" while parent claim 2 includes a "voltage divider coupled to said at least one time reference RS232 receiver" and not the "at least one RS232 receiver". Therefore, it is unclear to one having ordinary skill in the art as to what "voltage divider" is being referred.

Claim 16 is considered to be vague and indefinite because on line 13, reference is made to "the microprocessor". Claim 16, however, does not contain a previous mention of any "microprocessor" but instead describes a "signal detection circuit". Therefore, it is unclear to one having ordinary skill in the art as to whether "the microprocessor" refers to the "signal detection circuit" or some other unknown circuit.

Claims 17-20 are rejected under 35 U.S.C. 112, second paragraph, because they incorporate the lack of clarity present in parent claim 16.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-5, 12-14, and 16-20, as may best be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,272,427 to Nold et al. in view of U.S. Patent No. 5,841,992 to Martin.

Nold discloses an interface circuit comprising at least one microprocessor operable to perform one or more functions (column 4, lines 55-58), said microprocessor including at least a time input terminal for receiving a constant time reference AC voltage signal (column 4, lines 50-54 and column 6, lines 6-8) and a signal input terminal for receiving an AC input signal within a detectable microprocessor operating level (column 4, lines 17-27), a voltage divider coupled to said time input terminal to reduce the voltage of the constant time reference AC voltage signal to within a detectable range (column 4, lines 50-54) and a voltage divider coupled to said signal input terminal to reduce the incoming operational voltage to within a detectable range (column 4, lines 18-27) such that said microprocessor is operable to detect a change of state in said AC voltage input signal (column 5, lines 56-61 and column 6, lines 6-22). Nold further discloses that the at least one microprocessor is operable to be interrupted at a falling edge of the time reference signal (column 6, lines 6-11) and further a circuit operable to take a reading in response to said microprocessor being interrupted by said falling edge of said time reference signal (column 3, lines 34-47 and column 5, lines 56-61 and column 6, lines 11-22), wherein said interface circuit is coupled to at least one external controller selected from a group comprising a thermostat, a switch, a relay contact, and a humidity controller (column 5, lines 56-61).

Nold also discloses a method for detecting a state of an alternating current AC voltage control signal comprising providing an interface circuit including a microprocessor (column 4, lines 55-58) splitting a received input signal into a first and second signal (column 4, lines 1-17), and applying an AC voltage control signal as the first signal to a time input of said microprocessor (column 4, lines 50-54 and column 6, lines 6-8), and applying the AC voltage control signal as the second signal being coupled to a signal detection circuit (column 4, lines 17-27), obtaining a sampling time through detecting the first signal, interrupting said microprocessor in response to detecting the first signal, and sampling (i.e. reading) an output of the signal detection circuit a predetermined delay after interrupting the microprocessor to determine a state of the AC voltage control signal (column 5, lines 56-61 and column 6, lines 6-22).

Nold discloses activating a controller circuit to perform a predetermined function when the AC voltage control signal is determined to have a first state, wherein the predetermined function comprises activating a load circuit (column 3, lines 34-41) and the step of activating a controller circuit comprises activation of one of a relay, a switch, or a driver circuit (column 3, lines 5-11).

Nold further discloses the AC voltage control signal is produced by any of a plurality of external controllers (i.e. thermostat, high limit control, ignition control, and gas valve) (abstract).

As noted above, the invention of Nold teaches many of the features of the claimed invention and while the invention of Nold does teach a microprocessor

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having a signal input terminal and a time input terminal, wherein the microprocessor is a ULN2003A microprocessor that comprises TTL inputs (see ULN2003A Datasheet), Nold does not specifically include a corresponding means for insuring that the inputs are in TTL format.

Martin teaches a network-to-serial device intelligent converter comprising means for interfacing a network device to any one of several different types of serial devices (column 3, lines 38-40) communicating over a protocol commonly used for HVAC systems (column 1, lines 57-60) including an RS-232 receiver having an input for receiving an input signal and an output for transmitting a microprocessor logic operating voltage signal, the output of the RS-232 receiver being coupled to a signal input terminal of a microprocessor (column 6, lines 30-41).

It would have been obvious to one having ordinary skill in the art to modify the invention of Nold to specifically include RS-232 receivers on the input lines to the microprocessor, as taught by Martin, because, as suggested by Martin, the combination would have provided a corresponding means for insuring that the inputs to the microprocessor of Nold, receives input signals in the required, and accurately defined, format for operating the microprocessor using the TTL operation, as desired for providing defined logic levels rather than indistinct voltage levels (column 6, lines 30-41). Also, since the modification is to convert the AC voltage input signal and the time reference signal of Nold to TTL logical inputs using the RS-232 receivers of Martin, one having ordinary skill in the art would recognize that the output of the RS-232 receivers is based on the input to the RS-232 receivers.

Although the combination of Nold and Martin does not specifically disclose the use of twelve RS232 receivers, the invention of Nold and Martin does teach a plurality of external controllers each providing inputs to a microprocessor with an associated RS232 for each input to convert the data to a proper microprocessor format. It would have been an obvious modification to one having ordinary skill in the art to provide as many inputs as needed, such as twelve, in order to provide sufficient monitoring of all of the desired external controllers. Such a modification would also provide twelve corresponding RS232 receivers to provide the necessary conversion for the twelve inputs, as taught by the combination of Nold and Martin.

6. Claims 6-11, as may best be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nold et al. in view of Martin and further in view of U.S. Patent No. 5,321,323 to Lehmann.

As noted above, the invention of Nold and Martin teaches many of the features of the claimed invention including voltage dividers to step down the inputs to the microprocessor as well as converting the input to the microprocessors into a corresponding TTL voltage. The combination, however, does not specifically indicate the corresponding range of values required to conform to the TTL format.

Lehmann teaches a surge limited low-power transceiver circuit including RS-232 and TTL interfaces (column 2, lines 3-6) wherein the corresponding input range of the TTL system requires that the incoming operational voltage is between about .5 to 2.7 volts with an input logic high threshold voltage at about 2.1 volts (i.e. 2.0 volts)

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and an input logic low threshold voltage at about 1.1 volts (i.e. .8 volts) (column 3, lines 37-42), wherein the output of the interfaces is operable to switch to a logic high output when the input exceeds the input logic high threshold voltage and to switch to a logic low output when said input falls below the input logic low threshold voltage (column 4, lines 2-4).

It would have been obvious to one having ordinary skill in the art to modify the invention of Nold and Martin to specify that the incoming operational voltage be between about .5 to 2.7 volts with an input logic high threshold voltage at about 2.1 volts and an input logic low threshold voltage at about 1.1 volts, as taught by Lehmann, because the combination of Nold and Martin does teach transforming the input to the microprocessor to a TTL format and Lehmann suggests that a TTL format requires the incoming operational voltage be between about .5 to 2.7 volts with an input logic high threshold voltage at about 2.1 volts and an input logic low threshold voltage at about 1.1 volts (column 3, lines 37-42) and therefore the modification would have conformed to the requirements of the TTL format to insure accurate data detection by the microprocessor.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nold et al. in view of Martin and further in view of U.S. Patent No. 4,283,007 to Bramow et al.

As noted above the invention of Nold and Martin teaches many of the features of the claimed invention and while the invention of Nold and Martin does teach

including several safety features, the combination does not specifically include a failsafe interface control circuit coupled between an output terminal of an external controller and said input of said at least one RS232 receiver, whereby said failsafe interface control circuit is capable of minimizing microprocessor malfunctioning.

Bramow teaches multiple load integrated fluid control units in a VAC system (column 1, lines 9-13) including a controller for receiving inputs from a plurality of external controllers (column 2, lines 1-5) a failsafe interface control circuit (i.e. interlock circuit) coupled between an output terminal of an external controller and said input of the controller (column 2, lines 10-14 and column 11, lines 1-7), whereby said failsafe interface control circuit is capable of minimizing microprocessor malfunctioning (column 10, lines 13-29).

It would have been obvious to one having ordinary skill in the art to modify the invention of Nold and Martin to specifically include a failsafe interface control circuit, as taught by Bramow, because, as suggested by Bramow the combination would have improved the HVAC system operation of Nold and Martin by insuring that the microprocessor provided proper control during all conditions (column 12, lines 33-45) through proper temperature compensation as well as provide safety interlocking (column 10, lines 13-29).

Further, since the invention of Bramow teaches a failsafe interface control circuit coupled between an output terminal of an external controller and an input to a microprocessor and the invention of Nold and Martin teaches including an RS232 receiver between the external controller and microprocessor, the combination would

have provided the failsafe interface control circuit coupled between an output terminal of an external controller and said input of said at least one RS232 receiver.

Response to Arguments

8. Applicant's arguments filed January 30, 2006, have been fully considered but they are not persuasive.

Applicant argues:

The invention claimed in claim 1 is clearly distinguishable from *Nold* and *Martin* and other combinations of references used by the Examiner to reject the claims.

Martin merely describes a well-known use of an RS232 receiver in serial data communications for receiving transmitted digital signals. *Martin* neither teaches nor suggests use of the RS232 receiver to conditioning a sinusoidal AC voltage input signal for input to a microprocessor at a logic operating voltage level such that the microprocessor is operable to detect a change of state in the AC voltage input signal.

The purpose of the system described in *Nold* is to synchronize a microprocessor to an AC voltage power line (see, e.g., col. 1, Ins. 55-62). In the system described in *Nold* an AC voltage wave (e.g. the 24 VAC transformer common voltage) is applied to an interrupt input (IRQ input) without first converting an AC voltage to a microprocessor operating logic level (col. 6, Ins. 6-8).

Moreover, neither *Lehmann* nor *Bramow* supply the teaching which *Nold* and *Martin* lack with respect to the invention recited in claim 1. Clearly, none of the cited references teaches or suggests use of RS232 receivers for signal conditioning between AC voltage signals and input terminals of a microprocessor as recited in claim 1.

The Examiner asserts that the invention of *Martin* is not included to teach or suggest use of RS232 receivers for signal conditioning between AC voltage signals and input terminals of a microprocessor, but is only included to teach an RS-232 receiver having an input for receiving an input signal and an output for transmitting a

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microprocessor logic operating voltage signal, the output of the RS-232 receiver being coupled to a signal input terminal of a microprocessor (column 6, lines 30-41):

The RS-232 interface circuit 81 will convert the RS-232 voltage level signals to TTL level and pass the serial data to the microprocessor 74. The microprocessor 74 buffers the data (the internal UART may be used for this purpose) and then, on the basis of the data conversion routine associated with the particular serial device attached, feeds the data over parallel bus 75 to the Neuron® chip 72. The Neuron® chip 72, under program control, performs the necessary network (e.g., Lonworks™) protocol multi-layered operations and, when appropriate, will output the data, in packet form, via converter transceiver circuit 71 and lines 52, to the engine analyzer MPU 51, which processes the data.

The Examiner also asserts that Nold teaches applying AC voltage signals to input terminals of a microprocessor by splitting a received input signal into a first and second signal, the first signal being coupled to a time input of said microprocessor, the second signal being coupled to at least one external controller circuit (column 4, lines 1-27):

Turning now to FIG. 2 a schematic representation is shown of a control circuit made in accordance with the invention along with other components of a gas furnace system with which the control circuit is used. Transformer 10, providing 24 volts AC from line voltage, is connected at the 24 VAC output side to connector Q11 and then through a 5 amp fuse F1 to a full wave bridge comprising diodes CR1, CR1, CR3 and CR4. The transformer common is connected to the bridge through connector Q12. The bridge provides full wave rectified 24 VAC power to drive relays K1, K2 and K3 to be discussed below. Zener diode CR7 suppresses back EMF. Capacitor C2, resistor R15 and capacitor C1, resistor R1 provide 5 volts DC on line VDD for the power supply of microprocessor U2 to be discussed below.

There are several low voltage AC input terminals labeled Y1, Y2, C, G, R, W1, W2 and ECON. Terminals Y1, Y2 are not used in the present embodiment. Terminal C is connected to the transformer common, terminal G is coupled to an output of room thermostat 32 and to input port 3 of microprocessor U2 through a 100K ohm resistor R3 and is connected to common through pull down resistors R12, R13, R14 of 1.5 ohms connected in parallel to provide an equivalent resistance of 500 ohms.

Therefore, the combination of Nold applying AC voltage signals to input terminals of a microprocessor with Martin's teaching of an RS-232 receiver having an input for receiving an input signal and an output for transmitting a microprocessor logic operating voltage signal, the output of the RS-232 receiver being coupled to a signal input terminal of a microprocessor, meets the claim limitation in question of "use of RS232 receivers for signal conditioning between AC voltage signals and input terminals of a microprocessor".

The Examiner further asserts that the invention of Nold specifically indicates that the microprocessor that receives the AC voltage signals is a Texas Instruments ULN 2003A microprocessor (column 10, lines 3-4).

Turning to the supplied datasheet for the Texas Instruments ULN2003A microprocessors, the datasheet indicates that the inputs for the ULN2003A microprocessor are TTL compatible.

Therefore, one having ordinary skill in the art would recognize that in order to use the TTL inputs of the ULN2003A microprocessor disclosed in Nold, some type of conversion of the microprocessor inputs from AC to TTL is required. Consequently, one having ordinary skill in the art would be motivated to add Martin's teaching of RS-232 receivers to convert input signals to TTL format to Nold's teaching of inputting AC input signals to TTL-inputs of a microprocessor and, as such, meets the invention as claimed.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

U.S. Patent No. 5,640,153 to Hildebrand et al. teaches an energy utilization controller and control system and method for use in a HVAC system comprising RS-232 to TTL conversion.

U.S. Patent No. 6,266,001 to Fang et al. teaches a method and apparatus for switching low voltage CMOS switches in high voltage digital to analog converters wherein the input range for TTL logic is between .8 to 2.0 volts.

U.S. Patent No. 6,089,310 to Toth et al. teaches a thermostat with load activation detection failure.

U.S. Patent No. 6,450,409 to Rowlette et al. teaches a method and apparatus for a wiring room thermostat to two-stage HVAC system.

U.S. Patent No. 6,307,464 to Miller et al. teaches a method and apparatus using phases for communication in a thermostat circuit.

"ULN2003A" Datasheet teaches the use of TTL compatible inputs for the ULN2003A microprocessor.

Lux, "Voltage Dividers" teaches various forms of voltage dividers.

10. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

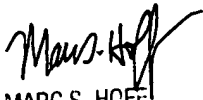
11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jrw
April 13, 2006


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